

**AMENDMENTS TO THE CLAIMS**

1. (Previously presented) A flash memory device comprising:
  - a semiconductor substrate;
  - a doped well within said semiconductor substrate;
  - a word line;
  - a bit line;
  - a plurality of array ground lines;
  - a plurality of flash memory transistors each having a respective source, drain, and control gate, each source being connected to a respective one of said plurality of array ground lines, each drain being coupled to said bit line, and each control gate being coupled to said word line; and
  - a plurality of coupling transistors spaced within said doped well, said coupling transistors each having a first terminal coupled to one of said array ground lines and a second terminal coupled to said doped well, said coupling transistors adapted to switchingly electrically couple said plurality of array ground lines to said doped well.
- 2-19. (Cancelled)
20. (Previously presented) The flash memory device of claim 1, wherein said plurality of coupling transistors are adapted to switchingly electrically couple said plurality of array ground lines to said doped well during a read cycle of said flash memory device.
21. (Previously presented) The flash memory device of claim 1, wherein said doped well comprises:
  - a p-well, said coupling transistors are n-type transistors, and each of said plurality of array ground lines includes a metallic trace.

22. (Previously presented) The flash memory device of claim 1 further comprising

a current sensing device including an analog to digital converter, said current sensing device having a first input coupled to a source of electric potential, a first output coupled to said bit line, and an output port adapted to output a digital value corresponding to a current flowing through said first output.

23. (Previously presented) The flash memory device of claim 1 further comprising a switching device adapted to switchingly couple said doped well and each of said plurality of array ground lines to a source of substantially constant potential.

24. (Previously presented) The flash memory device of claim 23 wherein said source of substantially constant potential comprises a source of ground potential.

25. (Previously presented) The flash memory device of claim 1 wherein said doped well comprises a p-well and wherein said plurality of flash memory transistors includes a plurality of n-type flash memory transistors, each of said flash memory transistors including a respective control gate and a respective floating gate.

26. (Previously presented) The flash memory device of claim 1 further comprising:

a grounding transistor coupled between each of said plurality of array ground lines and a source of ground potential.

27. (Previously presented) The flash memory device of claim 1 wherein said doped well is adapted to assume an electrical potential equal to one threshold voltage of said plurality of coupling transistors during a time interval when said coupling transistors are in a conductive state.

28. (Previously presented) The flash memory device of claim 1, wherein:  
said doped well includes a p-type semiconductor well and said substrate includes a p-type semiconductor substrate; and  
wherein said memory device includes a region of n-type semiconductor material disposed between said doped well and said substrate.

29. (Previously presented) The flash memory device of claim 1 wherein said plurality of coupling transistors are responsive to a control signal having a first state adapted to make said coupling transistors non-conductive during a device erasing time interval and a second state adapted to make said coupling transistors conductive during a device reading time interval.

30. (Previously presented) A flash memory device comprising:  
a semiconductor substrate;  
a doped well within said semiconductor substrate;  
a word line;  
a bit line;  
a plurality of array ground lines;  
a plurality of flash memory transistors each having a respective source, drain, and control gate, each source being connected to a respective one of said plurality of array ground lines, each drain being coupled to said bit line, and each control gate being coupled to said word line; and

a plurality of coupling transistors spaced within said doped well, said coupling transistors each having a first terminal coupled to one of said array ground lines and a second terminal coupled to said doped well, said coupling transistors adapted to switchingly electrically couple said plurality of array ground lines to a region of said substrate outside of said doped well.

31. (Previously presented) The flash memory device of claim 30, wherein:  
said doped well includes a p-type semiconductor well and said substrate includes a p-type semiconductor substrate; and  
wherein said memory device includes a region of n-type semiconductor material disposed between said doped well and said substrate.

32. (Previously presented) The flash memory device of claim 30 further comprising a grounding transistor coupled between each of said plurality of array ground lines and a source of ground potential.

33. (Previously presented) The flash memory device of claim 30, wherein said doped well is adapted to assume an electrical potential equal to one threshold voltage of said plurality of coupling transistors during a time interval when said coupling transistors are in a conductive state.

34. (Previously presented) A system comprising:  
a processor;  
at least one flash memory device coupled to exchange data with said processor,  
said at least one flash memory device comprising:  
a doped well within a semiconductor substrate;

a word line;

a bit line;

a plurality of array ground lines;

a plurality of flash memory transistors each having a respective source, drain, and control gate, each source being connected to a respective one of said plurality of array ground lines, each drain being coupled to said bit line, and each control gate being coupled to said word line; and

a plurality of coupling transistors spaced within said doped well, said coupling transistors each having a first terminal coupled to one of said array ground lines and a second terminal coupled to said doped well, said coupling transistors adapted to switchingly electrically couple said plurality of array ground lines to said doped well.